IN THE SPECIFICATION

Please replace the paragraph at page 34, lines 14-26, with the following rewritten paragraph:

As shown in FIG. 56, an n^+ diffusion layer (impurity layer) 202 at the trench bottom is so patterned as to be made in a one-half overlapped relation to many silicon columns. By doing so, it is possible to connect all associated silicon columns 201 in a shared relation to the n^+ diffusion layer 202 (for example, see FIGS. 45A, [[and]] 45B, 46A and 46B). In the case where, however, the diffusion resistance is greater than the ON resistance of the transistor, a memory write-in/read-out rate will be slower due to the diffusion resistance. In this case, the number of parallel-connected silicon columns 201 may be restricted to, for example, five or ten per contact.

Please replace the paragraph beginning at page 36, line 18, through page 37, line 2, with the following rewritten paragraph:

Even if there is a size error in the same chip, the same light exposure is made at a light exposure time after movement under the use of the same mask and there is less error involved. By repeating this method a multiple of times, it is possible to theoretically obtain a cell size of F^2, $0.5F^2$. At this time, at the both ends on the diagonal line (shown by dashed line) 90° orthogonal to a moving direction at the light exposure time of the memory cell array, no memory cell is patterned (at a site x in FIG. 57B). Thus, uppermost/lowermost or rightmost/leftmost lines of the memory cell arrays may be used as dummy patterns.